Remarks

The foregoing amendments and these remarks are in response to the Office Action dated January 16, 2004.

Claims 1 – 6 are amended, claim 7 is cancelled without prejudice and claims 8 – 13 are added.

The specification is amended to include reference indicia CS1 and CS2 shown in drawing figure 2 and to correct a typographic error. No new matter has been added.

Prior to addressing the Examiner's rejections on the art, a brief review of applicant's invention is appropriate. The invention relates to a variable conduction device that is coupled to a scanning velocity modulation (SVM) deflection signal generator that includes a transistor having two signal inputs. For instance, the transistor is operable both as a common emitter amplifier and as an amplifier configured for common base operation. One of the transistor input electrodes (emitter) is responsive to a feed back signal representative of the SVM deflection signal, and the other input electrode (base) is responsive to a control signal. In a first condition, the transistor receives the feedback signal and provides a feedback path for controlling the magnitude of the SVM deflection signal. In a second condition, the control signal causes the transistor to interrupt the feedback path and inhibit generation of the SVM deflection signal by attenuating the input signal fed to the SVM amplifier. Accordingly, the variable conduction device not only controls the magnitude of the SVM deflection signal by means of negative feedback, but in addition turns the deflection signal on or off using just a single transistor, thus controlling the SVM deflection signal at minimum cost.

Claim Rejections on the Art

At the time of the Office Action, claims 1-7 were pending in the application. Claims 1-3 and 6-7 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,072,300 to Anderson ("Anderson") and claims 4 - 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson.

Anderson provides a circuit for selectively disabling normal SVM circuit operation when an on screen display generator is being used. Importantly, Anderson discloses the use of four transistors 65, 118, 133 and 136 for implementation of his SVM solution.

Amended claim 1 recites a generator of a scanning velocity modulation deflection signal comprising a variable conduction device that itself comprises a single transistor (Q1). The transistor has a first input (Q1e) responsive to a negative feedback signal CS1 representative of scanning velocity modulation deflection power, and a second input (Q1b) responsive to a control signal CS2. Anderson fails to teach or suggest this limitation. In particular, Anderson's multiple transistors each have only a single input which is responsive to a signal. In consequence, Anderson must utilize a greater number of transistors and associated components to control the SVM deflection signal. Indeed, as noted, Anderson uses four transistors to implement his solution, which is not only more costly than the claimed device but in addition reduces component reliability. Thus, Anderson's use of a greater number of transistors increases the likelihood of component failure as compared to the circuit of the present invention.

Claims 2 – 6 depend from claim 1 and are, for the same reasons not anticipated by Anderson.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Anderson in view of the Examiner's Official Notice.

With respect to claims 4 and 5 the Examiner takes Official Notice that applicant's use of a fully conductive device for inhibiting during a second condition is well known. Applicant respectfully disagrees.

Although the use of variable conduction states is known, applicant's inventive arrangement substantially inhibits generation of the scanning velocity modulation deflection signal in a manner (by saturated conduction of transistor Q1) which is completely contrary to the action of Anderson where transistor 65 is turned <u>off</u> to inhibit signal generation. Furthermore when transistor 65 of Anderson is fully conductive the SVM deflection signal is <u>maximized</u> not inhibited. Anderson offers no motivation to one of ordinary skill to modify the circuitry to provide applicant's recited signal inhibition by use of a fully conductive device. In addition, Anderson

offers no teaching nor motivation to enable one of ordinary skill to modify Anderson's arrangement to provide the recited features of applicant's claims 4 and 5.

New Claims

Claims 8 and 9 have been added to recite features of applicant's invention which are believed allowable. No new matter has been added.

Specifically, claim 8 recites a variable conduction device consisting of a single transistor (Q1) having a first input (Q1e) responsive to a scanning velocity modulation feedback signal, and a second input (Q1b) responsive to a control signal. Notwithstanding that Anderson's transistors each have a single signal input, as noted, Anderson's circuitry for turning on and varying the SVM deflection signal utilizes four transistors, namely transistors 65, 118, 133, 136.

Claim 9 recites a scanning velocity modulation deflection signal generator that comprises a transistor (Q1) which is operational both as a common emitter amplifier and as a common base amplifier. The common base amplifier is used to provide a feedback path, from emitter to collector, for controlling the magnitude of the scanning velocity modulation deflection signal (Vm). The common emitter configuration uses the transistor base to controllably interrupt the common base feedback path (Q1e Q1c) and thus inhibit generation of the scanning velocity modulation deflection signal (Vm). Anderson does not teach nor suggest the use of a transistor configured as applicant's claim 9 for selectable operation as either a common emitter or common base amplifier. Indeed, each of Anderson's transistors 65, 118, 133, 136 only operate in a common emitter configuration.

New claim 10 depends from claim 1, claim 11 depends from claim 8, and claims 1 and 13 depend from claim 9.

Although Anderson's teachings are directed to objectives similar to applicant's, their respective circuit solutions are significantly different. Applicant's novel circuit arrangement using a single transistor to perform dual functions is not

shown nor suggested by Anderson and is therefore considered patentable over Anderson's teachings. Applicant respectfully requests the withdrawal of the rejection of claims 1 - 6 and their allowance together with the allowance of newly added claims 8 - 13.

Respectfully submitted,
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